

WHAT IS CLAIMED:

1. A receiver for high speed data interconnect, comprising:
 - a sampling system comprising at least one sampler for sampling data, for providing a series of signal copies, each signal copy having a Bit Error Rate Distribution;
 - a means to combine the signal copies so as to produce a combined signal having the Bit Error Rate Distribution narrower than the distribution of a single signal copy.
2. A receiver according to claim 1, wherein the sampling system comprises a plurality of samplers producing a series of copies simultaneously.
3. A receiver according to claim 1, wherein the sampling system comprises at least one sampler coupled to a set of delays or a variable delay, for providing a series of spaced in time signal copies.
4. A receiver according to claim 1, wherein the sampling system comprises a plurality of samplers coupled to a set of delays, for providing a plurality of spaced in time signal copies.
5. A receiver according to claim 1, wherein the means for combining signal copies comprises a logic network that compares the values of bit errors relative to each signal copy, and a means for selecting the signal copy with the minimum Bit Error Rate.
6. A receiver according to claim 1, wherein the signal copies are spaced in time by fixed delays.
7. A receiver according to claim 1, wherein the signal copies are spaced in time by variable delays.
8. A receiver according to claim 1, wherein the signal copies are spaced in time uniformly.

9. A receiver according to claim 5, wherein the logic network comprises at least one majority element for providing a value Q, where Q is the value at the majority of its inputs, and a number E, where E is the number of its inputs having value different from the value at the majority of inputs.

5 10. A receiver according to claim 3, further comprising a means to determine the bit errors against the delay, a means to determine the delay corresponding to a copy with minimal bit error and a means to apply the delay determined thereby to other samplers.

10 11. A receiver according to claim 1, wherein the sampler is implemented as register, flip-flop, latch, sample-hold, or track-and-hold device.

12. A receiver according to claim 1, wherein the sampler latches data at a point where the BER function has its minimum.

13. A receiver according to claim 1, further comprising a pipeline of latency adjustment elements.

15 14. A receiver according to claim 3, wherein said delay elements are incorporated in a data path, in a clock signal path, or in both paths.

15. A receiver according to claim 9, wherein the minimum number of inputs at the majority element is 3.

20 16. A receiver according to claim 1, wherein the number of samplers per bit is from 14 to 20, preferably, 16.

17. A receiver according to claim 1, wherein at least one signal copy from the sampler is used to generate a feedback to control a source of threshold voltage to balance the number of ones and zeros in the sampled data.

18. A method of high speed data interconnect, comprising the steps of:

25 - sampling data using at least one sampler, for providing a series of signal copies, each signal copy having a Bit Error Rate Distribution;

- combining the signal copies so as to produce a combined signal having the Bit Error Rate Distribution narrower than the distribution of a single signal copy.

19. A method according to claim 18, wherein a series of simultaneous signal copies is provided.

20. A method according to claim 18, wherein a series of spaced in time signal copies is provided.

21. A method according to claim 18, wherein the step of combining signal copies comprises:

- comparing signal copies to determine the number of a signal copy with minimal BER, and
- selecting the signal copy with minimal BER.

22. A method according to claim 18, wherein the data are sampled at a point where the BER function has its minimum.

23. A method according to claim 20, wherein the spaced in time signal copies are produced by using a set of delays or a variable delay, the step of combining signal copies comprises determining the bit errors against the delay and determining the delay corresponding to a copy with minimal bit error; wherein the step of sampling data is performed at a time corresponding to the delay determined thereby.

24. A method according to claim 18, wherein the minimum number of inputs at majority elements is 3.

25. A method according to claim 18, wherein the number of samplers per bit is from 14 to 20, preferably, 16.

26. A method according to claim 18, wherein the data is transmitted along a communication channel comprising a plurality of parallel buses, on which a plurality of receivers is arranged.

27. A method according to claim 18, further comprising a step of adjusting latency using a pipeline of latency adjustment elements.

28.A method according to claim 27, wherein initial pipeline values are updated during initialization procedure to provide the same latency on each bit.

29.A communication channel employing a receiver according to claim 1.

5 30.A communication channel as claimed in claim 29, wherein the number of samplers per bit is from 14 to 20, preferably 16.

31.A communication channel according to claim 29, comprising a plurality of parallel buses, on which a plurality of receivers as claimed in claim 1 is arranged.

10 32.A communication channel according to claim 31, wherein each receiver comprises a pipeline of latency adjustment elements.

33.A receiver according to claim 32, wherein initial pipeline values are updated during initialization procedure to provide the same latency on each bit.

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